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EXAMINER	
ROMAN, LUIS ENRIQUE	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,366	BLUMENAUER ET AL.	
	Examiner	Art Unit	
	Luis Roman	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/09/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,9,11-14,16,17,23-28,30-36,38-41 and 43-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *8, 9, 11-14, 16, 17, 23, 24-28, 30-36, 38-41, 43-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant amendment filed on 01/09/06 has been entered. Accordingly claims 8, 9, 13, 14, 16, 17, 23, 24, 30, 33, 34 & 41 have been amended and claims 1-7, 10, 15, 18-22, 29, 37 & 42 have been cancelled. New claims 43-58 were added. It also included remarks/arguments.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 9, 11, 12, 13, 24, 25, 26, 30, 31, 32, 33, 34, 35, 36, 38, 39, 43, 52 & 53 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bereskin (US 4159499).

Regarding claim 8 Bereskin discloses a ground and line fault interrupter (Abstract, first paragraph) comprising: a magnetic core (Fig. 1 element 36) wherein load wires of a three-phase electric circuit extend through said magnetic core (Fig. 1 elements 36, 20, 20a, 20b), and wherein said magnetic core is capable of detecting a magnetic field from at least one fault current flowing through said load wires (Col. 2 lines 49-52 & Fig. 4); multiple conductive windings (Fig. 1 elements 22w, 38) with a first output and a second output voltage (Col. 1 lines 24-32<teachings of having more than one circuit to detect different faults>), and being magnetically coupled to said magnetic core (Fig. 1 element 22w, 38) wherein said first output is directly proportional to a ground fault level (It is obvious that a ground fault is a synonymous of a return current whether is through the neutral or ground line), and wherein said second output is

directly proportional to a line fault level (Fig. 3<v-i characteristics of diodes 40a, 40b which are proportional for the most part> or Fig. 5 element 40' <which will make it proportional>); a first sensing circuit being electrically connected to said multiple conductive windings and monitoring said first output voltage, wherein said first sensing circuit detects ground fault conditions between at least one of said load wires and ground (Col. 1 lines 5-9); a second sensing circuit being electrically connected to said multiple conductive windings and monitoring said second output voltage, wherein said second sensing circuit detects line fault conditions between at least two of said load wires (Col. 1 lines 5-9); and a printed wiring board circuit breaker being electrically connected to an output of said first sensing circuit and an output of said second sensing circuit (Fig. 1 element 46<Col. 3 lines 12-13 intrinsically teaches about a electronic board>), wherein said printed wiring board circuit breaker (Fig. 1 element 46) receives a ground fault condition signal from said first sensing circuit or a line fault condition signal from said second sensing circuit (Fig. 1 element 22w) wherein said printed wiring board circuit breaker is tripped and generates an electronic fault signal when at least one of said received fault condition signals exceeds a preset threshold (Col. 8 lines 59-68); and wherein said electronic fault signal activates an external circuit breaker system that is electrically connected to said three-phase system (Fig. 1 elements 42, 44, 46 & 20, 20a, 20b).

Bereskin does not specifically disclose a first sensing circuit being electrically connected to said multiple conductive windings and monitoring said first output voltage, wherein said first sensing circuit detects ground fault conditions between at least one of said load wires and ground and second sensing circuit being electrically connected to said multiple conductive windings and monitoring said second output voltage.

Bereskin teaches about prior art using separated circuits for different fault detection (Col. 1 lines 24-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the teachings of having two separated detecting circuits or just duplicate the existing one for each of the fault detections. This way the magnetic circuit can be cheaper and simplified.

Regarding claim 9 Bereskin discloses the module of claim 8.

Bereskin further discloses wherein each of said first and second sensing circuits includes: an impedance with a first terminal and a first opposed terminal, the first terminal of said impedance being electrically connected to of said multiple conductive windings, wherein said impedance is a load that provides a voltage drop in said first or second output voltages (Col. 7 lines 7-18 & Figs. 1 element 40 and 5 element 40'<Col. 1 lines 24-32, teachings of having more than one circuit to detect different faults, and as a result provide two voltages>); a rectifier with a second terminal and a second opposed terminal, the second terminal of said rectifier being electrically connected to the first opposed terminal of said impedance, wherein said rectifier rectifies said dropped voltage (Col. 8 lines 47-54 & Fig. 2 elements D4, R13, R14); an electronic filter with a third terminal and a third opposed terminal, the third terminal of said electronic filter being electrically connected to the second opposed terminal of said rectifier (Col. 8 lines 54-58 & Fig. 2 elements C6, R13, R14, R15); wherein said filter characteristics are adjusted to balance a trip time with a number of false trips (each determined set of resistors-capacitors will have a different cut-off frequency), and wherein said filter filters said dropped voltage; and a comparator with a fourth terminal and a fourth opposed terminal, the fourth terminal of said comparator being electrically connected to the third opposed terminal of said electronic filter (Col. 8 lines 59-68 & Fig. 2 elements TR9, TR10, TR11), the fourth opposed terminal of said comparator being electrically connected to the input of said printed wiring board circuit breaker (Col. 3 lines 12-13<intrinsically disclosed a board circuit>).

Regarding claim 11 Bereskin discloses the module of claim 9.

Bereskin further discloses wherein said three phase circuit includes at least one switch (Fig. 1 element 46) capable of receiving the electronic fault signal (Col. 3 lines 63-68).

Regarding claim 12 Bereskin discloses the module of claim 11. Bereskin further discloses wherein said three phase circuit is electrically connected to at least one load impedance (Col. 1 lines 11-15 & Fig. 1 element 24) through said at least one switch (Fig. 1 element 46).

Regarding claim 13 Bereskin discloses the module of claim 12. Bereskin further discloses wherein said three phase circuit (Fig. 1 elements 11, 11a, 11b) and said at least one load impedance (Col. 1 lines 11-15 & Fig. 1 element 24) are electrically connected through a conductive interconnect (Fig. 1 elements 20W, 20aW, 20bW) which extends through said magnetic core (Fig. 1 element 36), said conductive interconnect being electrically connected in series with said at least one switch (Fig. 1 element 46).

Regarding claim 24 Bereskin discloses a method (a person of the ordinary skill will understand a method that is intrinsically described by the functioning of the apparatus) of detecting an electronic fault in a circuit (Abstract), the method comprising the steps of: detecting a magnetic field from a fault current flowing through a switch in said circuit (Abstract & Fig. 1 element 22w), using a magnetic core (Fig. 1 element 36) and multiple conductive windings arranged on said magnetic core (Fig. 1 elements 22w, 38) converting said fault current into a ground fault signal and a line fault signal; measuring the ground fault signal by comparing the ground fault signal to a ground fault reference, measuring the line fault signal by comparing the line fault signal to a line fault reference signal; constantly monitoring said fault signals (Col. 8 lines 59-68); tripping a circuit breaker detector if a least one of said ground and line fault signals exceeds a threshold (Col. 2 lines 22-34); generating an electronic fault signal; opening said switch with said generated electronic fault signal to create an open circuit when the ground fault signal is greater than or equal to the ground fault reference signal; and opening said switch to create an open circuit when the line fault signal is greater than or equal to the line fault reference signal (Col. 6 lines 18-63).

Bereskin does not specifically disclose thresholds and signals greater than or equal to that value to trip the circuit breaker. However, Bereskin teaches a voltage sensor that is designed such that an electromagnetic actuator is actuated, tripping a circuit breaker, only when the decrease in voltage across a neutral winding drops to a level corresponding to a line conductor leakage path through resistor exceeding a certain value of current (Col. 6 lines 18-24).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the teachings of having two separated detecting circuits with their respective thresholds or just duplicate the one present for each one of the fault detections. This way the magnetic circuit can be cheaper and simplified.

Regarding claim 25 Bereskin discloses the method of claim 24.
Bereskin further discloses wherein said step of comparing the line fault signal to the line fault reference signal includes a step of measuring a voltage across an impedance (Col. 8 lines 59-68 & Col. 1 lines 24-32).

Regarding claim 26 Bereskin discloses the method of claim 24.
Bereskin further discloses wherein said steps of comparing the ground fault signal to the ground fault reference signal include a step of measuring a voltage across an impedance (Col. 8 lines 59-68 & Col. 1 lines 24-32).

Regarding claim 30 Bereskin discloses the method of claim 24.
Bereskin further discloses wherein said step of detecting the magnetic field with said magnetic device includes a step of inducing a current in said magnetic core (Col. 5 lines 30-40).

Regarding claim 31 Bereskin discloses the method of claim 24. Bereskin further discloses wherein said step of measuring the line and ground fault signals includes a step of rectifying at least one of the line and ground fault signals (Col. 5 lines 30-40).

Regarding claim 32 Bereskin discloses the method of claim 31. Bereskin further discloses wherein said step of measuring the line and ground fault signals includes a step of filtering at least one of the line and ground fault signals (Col. 8 lines 54-58).

Regarding claim 33 Bereskin discloses a method (a person of the ordinary skill will understand a method that is intrinsically described by the functioning of the apparatus) of detecting an electronic fault in a circuit (Abstract), the method comprising the steps of: providing a three phase circuit (Fig. 1 elements 11, 11a, 11b) electrically connected to an impedance (Col. 1 lines 11-15) through at least one conductive interconnect (Fig. 1 element 20W, 20aW, 20bW) and at least one switch (Fig. 1 element 46); measuring a current flowing through said at least one conductive interconnect to determine a ground fault signal and a line fault signal, comparing the ground fault signal with a ground reference current (Col. 8 lines 59-68); and generating an electronic fault signal if said ground fault signal or said line fault signal exceeds a preset threshold (Col. 2 lines 22-34); and opening said switch with said generated electronic fault signal to create an open circuit if the ground fault signal is greater than or equal to the ground reference current or if the line fault signal is greater than or equal to the line current. (Col. 6 lines 18-63).
Bereskin does not specifically disclose thresholds and signals greater than or equal to that value to trip the circuit breaker. However, Bereskin teaches a voltage sensor that is designed such that a electromagnetic actuator is actuated, tripping a circuit breaker, only when the decrease in voltage across a neutral winding drops to a level corresponding to a line conductor leakage path through resistor exceeding a certain value of current (Col. 6 lines 18-24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the teachings of having two separated detecting circuits with their respective thresholds or just duplicate the existing one for each of the fault detections. This way the magnetic circuit can be cheaper and simplified.

Regarding claim 34 Bereskin discloses the method of claim 33.
Bereskin further discloses wherein said step of measuring the current flowing through said at least one conductive interconnects includes measuring a magnetic field with multiple conductive windings (Fig. 1 elements 38 and 22W).

Regarding claim 35 Bereskin discloses the method of claim 34.
Bereskin further including a step of choosing the ground and line currents by choosing a number of turns in said multiple conductive windings (Col. 5 lines 51-55).

Regarding claim 36 Bereskin discloses the method of claim 33.
Bereskin further discloses wherein said step of comparing the ground fault signal with the ground reference signal and the line fault signal to the line reference signal includes a step of measuring a voltage across an impedance (Col. 8 lines 59-68 & Col. 1 lines 24-32).

Regarding claim 38 Bereskin discloses the method of claim 33.
Bereskin further discloses wherein said step of measuring the line and ground fault signals includes a step of rectifying at least one of the line and ground fault signals (Col. 8 lines 47-51).

Regarding claim 39 Bereskin discloses the method of claim 38.
Bereskin further discloses wherein said step of measuring the line and ground fault signals includes a step of filtering at least one of the line and ground fault signals (Col. 8 lines 54-58).

Regarding claim 43 Bereskin discloses a ground and line fault interrupter (Abstract), comprising: a magnetic core, wherein load wires of a three-phase system extend through said magnetic core (Fig. 1 element 36), said load wires providing three-phase power (Fig. 1 elements 11, 11a, 11b) to an electrical load (Col. 1 lines 11-15); multiple conductive windings wrapped around said magnetic core (Fig. 1 elements 22w, 38), wherein arrangement of said windings on said magnetic core enables monitoring of the current flow through said load wires and detection of imbalances in the current flow (Col. 2 lines 49-52 & Fig. 4), a first sensing circuit electrically connected to said conductive windings, wherein said first sensing circuit electronically monitors said conductive windings and detects imbalances in the current flow through said load wires that indicate ground fault conditions (Col. 1 lines 5-9), a second sensing circuit electrically connected to said conductive windings, wherein said second sensing circuit electronically monitors said conductive windings and detects imbalances in the current flow through said load wires that indicate line fault conditions (Col. 1 lines 5-9); and an analog operating circuit breaker detector electrically (Col. 2 lines 49-52 & Fig. 4) connected to said first and second sensing circuits, wherein said circuit breaker detector receives a fault current from said first and second sensing circuits, and wherein said circuit breaker detector is tripped and generates an electronic fault signal if said received fault current exceeds a preset threshold (Col. 8 lines 59-68).

Bereskin does not specifically disclose a first sensing circuit electrically connected to said conductive windings, wherein said first sensing circuit electronically monitors said conductive windings and detects imbalances in the current flow through said load wires that indicate ground fault conditions, a second sensing circuit electrically connected to said conductive windings, wherein said second sensing circuit electronically monitors said conductive windings and detects imbalances in the current flow through said load wires that indicate line fault conditions.

Bereskin teaches about prior art using separated circuits for different fault detection (Col. 1 lines 24-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the teachings of having two separated

detecting circuits or just duplicate the existing one for each of the fault detections. This way the magnetic circuit can be cheaper and simplified.

Regarding claim 52 Bereskin discloses the ground and line fault interrupter of Claim 43.
Bereskin further discloses including a power supply electrically connected to said conductive windings (Col. 2 lines 56-57 & Fig. 1 element 10).

Regarding claim 53 Bereskin discloses the ground and line fault interrupter of Claim 43.
Bereskin further implicitly discloses wherein said power supply is a 115 VAC system without external connections (Col. 2 lines 56-57 & Fig. 1 element 10<the most widely voltage for a VAC power supply with frequency 60 Hz and powering a machine tool is 115 VAC>).

Claims 14, 50 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bereskin (US 4159499) in view of Sid (US 6359761).

Regarding claim 14 Bereskin discloses the module of claim 8.
Bereskin does not specifically disclose wherein the output of said first sensing circuit is electrically connected to a first input of an OR gate and the output of said second sensing circuit is electrically connected to a second input of said OR gate wherein an output of said OR gate is electrically connected to the input of said printed wiring board circuit breaker.
Bereskin teaches the fault signal connected to the circuit breaker (Fig. 1 element 42a, 44 46) and prior art using separated circuits for different fault detection (Col. 1 lines 24-32).
Bereskin does not disclose the usage of an OR gate connected to the circuit breaker.
Sid teaches various types of fault connected to an OR gate (Abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the Sid teachings because the circuit outputs can be combined using a logical OR gate to cause specific actions in response to each detected fault, including terminating the high voltage generation in response to an excessive fault current.

Regarding claim 50 Bereskin discloses the ground and line fault interrupter of Claim 43.
Bereskin does not specifically disclose wherein the outputs of the comparators of the first and second sensing circuits are electrically connected to said circuit breaker detector through an OR gate.
Bereskin teaches prior art using separated circuits for different fault detection (Col. 1 lines 24-32).
Sid teaches various types of fault connected to an OR gate (Abstract).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the Sid teachings because the circuit outputs can be combined using a logical OR gate to cause specific actions in response to each detected fault, including terminating the high voltage generation in response to an excessive fault current.

Claim 27 is rejected under 35 U.S.C. §103(a) as being unpatentable over Bereskin (US 4159499) in view of Finlay, Sr. et al. (US 6980005).

Regarding claim 27 Bereskin discloses the method of claim 24.
Bereskin does not disclose wherein said step of opening said switch includes a step of flowing a ground fault current greater than one Amp through said switch.
Finlay, Sr. et al. teaches wherein said step of opening said switch includes a step of flowing a ground fault current greater than one Amp through said switch.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the Finlay, Sr. et al. teachings to have a device with a predetermined range, which allows it to trip only after certain value.

Claim 28 is rejected under 35 U.S.C. §103(a) as being unpatentable over Bereskin (US 4159499) in view of Tobin (US 6727682).

Regarding claim 28 Bereskin discloses the method of claim 24.
Bereskin does not disclose wherein said step of opening said switch includes a step of flowing a line fault current greater than 90 Amps through said switch.
Tobin teaches wherein said step of opening said switch includes a step of flowing a line fault current greater than 90 Amps through said switch (Col. 10 lines 15-20).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the Tobin teachings to have a device with a predetermined range, which allows it to trip only after certain value.

Claims 23, 41, 44, 46, 55, 57, 58 & 16 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bereskin (US 4159499) in view of Taniguchi et al. (US 5000692).

Regarding claim 23 Bereskin discloses a fault interrupter module (Col. 3 lines 12-13) comprising: a multiple conductive windings (Fig. 1 elements 22w, 38) providing a first and a second output voltage (Col. 1 lines 24-32<teachings of having more than one circuit to detect different faults>), said multiple conductive windings being magnetically coupled to said magnetic core (Fig. 1 elements 36, 22w, 38); first and second sensing circuits electrically connected to said multiple conductive windings (Col. 1 lines 5-9), said sensing circuits being capable of detecting a ground fault from the first output voltage of said multiple conductive windings and a line fault from the second output voltage of said multiple conductive windings; a analog operating circuit breaker detector electrically connected to said sensing circuits (Fig. 1 elements 42, 44, 46), said circuit breaker outputting an electronic fault signal when at least one of the ground and the line

faults are detected (Fig. 1 elements 46<"open" or "close" depending upon control signal>); and a relay module electromagnetically coupled with said electrical ground and line fault circuitry, (Fig. 1 elements 44<RELAY>), a relay socket module (see Taniguchi et al. below) electrically connected to external electrical circuitry; a ground and line fault interrupter adapter module (Abstract) fixedly attached to said relay socket module (see Taniguchi et al. below), said adapter module including a magnetic core (Fig. 1 element 36) capable of detecting a magnetic field from at least one fault current (Col. 2 lines 49-52 & Fig. 4), and said relay module being in electrical communication with said relay socket module through conductive interconnects extending through said relay module (see Taniguchi et al. below) including a switch electrically activated by the electronic fault signal (Fig. 1 element 46).

Bereskin does not specifically disclose first and second sensing circuits electrically connected to said multiple conductive windings, said sensing circuits being capable of detecting a ground fault from the first output voltage of said multiple conductive windings and a line fault from the second output voltage of said multiple conductive windings. However, Bereskin teaches about prior art using separated circuits for different fault detection (Col. 1 lines 24-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the teachings of having two separated detecting circuits or just duplicate the existing one for each of the fault detections. This way the magnetic circuit can be cheaper and simplified.

Bereskin does not disclose a relay socket module electrically connected to external electrical circuitry, being in electrical communication with the relay module through conductive interconnects extending through said relay module.

Taniguchi et al. teaches a relay socket module electrically connected to external electrical circuitry (Abstract), being in electrical communication with the relay module through conductive interconnects extending through said relay module (Col. 6 lines 33-45Fig. 6 elements 100, 101, 102, 30A).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the Taniguchi et al. device because it

provides an improved I/O relay interface module which is capable of being expanded to be connected to one or more additional relays for actuation or monitoring of correspondingly additional I/O devices under the control of a same central controller. Moreover, it is capable of being expanded to include additional relays which may be mounted on a like interface module or mounted separately on individual terminal blocks. The combination of the ground and line fault interrupter of Bereskin and the relay socket module of Taniguchi et al. turns into a ground and line fault interrupter adapter module.

Regarding claim 41 Bereskin discloses a method (a person of the ordinary skill will understand a method that is intrinsically described by the functioning of the apparatus) of providing electronic fault detection in a circuit (Abstract), the method comprising the steps of: providing at least one electrical circuit module in electrical communication with a connection in said circuit (Col. 2 lines 65-68), said at least one electrical circuit module including at least one electrical interconnect (Fig. 1 element s 11, 11a, 11b) and at least one switch (Fig. 1 element 46); removing said at least one first electrical circuit module from said connection in said circuit (Col. 2 lines 65-68).
Bereskin does neither specifically disclose an electrical circuit module, nor an electrical ground nor line fault indicator circuitry.
Taniguchi et al. teaches an electrical circuit module (Abstract).
Taniguchi et al. teaches an electrical ground and line fault indicator circuitry (Col. 6 lines 6-12 & Fig. 1 elements 33).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the Taniguchi et al. device because it reduces the space required in electrical control panels for mounting and interconnecting by means of electrical conductors various electrical components situated in these panels, as for example relays. Moreover, it provides an inexpensive plug-in device that monitors faults in the lines, interrupting the circuit and/or warns the user with visual signal indications.

The combination of the ground and line fault interrupter of Bereskin and the I/O relay interface module of Taniguchi et al. turns into a ground and line fault interrupter indicator and adapter modules mounting assembly.
Bereskin further discloses providing an adapter module which includes electrical ground and line fault indicator circuitry, said adapter module being positioned in said connection in said circuit, positioning said at least one electrical circuit module on said adapter module, generating an electronic fault signal with said electrical ground and line fault indicator circuitry (Col. 2 lines 22-34); transmitting a said electronic signal from said adapter module to said at least one switch (Col. 8 lines 59-68), and opening said at least one switch when said electronic fault signal is detected by said at least one switch (Col. 6 lines 18-63), said at least one electrical interconnect extending through said electrical ground and line fault indicator circuitry to make electrical contact with said circuit (Fig. 1 elements 46, 20, 20a, 20b), detecting a fault current flowing through said at least one electrical circuit module with said electrical ground and line fault indicator circuitry (Col. 1 lines 5-9).

Regarding claim 44 Bereskin discloses the ground and line fault interrupter of Claim 43.
Bereskin further discloses wherein said electronic fault signal generated by said circuit breaker detector trips a circuit breaker, that is electrically connected to said three-phase system (Fig. 1 elements 36, 42, 44, 46, 11, 11a, 11b).
Taniguchi et al. further discloses wherein the circuit breaker is an external circuit breaker system (Fig. 6).

Regarding claim 46 Bereskin discloses the ground and line fault interrupter of Claim 43.
Bereskin further discloses wherein said electronic fault signal generated by said circuit breaker detector trips a relay of an external relay system that is electrically connected to said three- phase system (Fig. 1 elements 36, 42, 44, 46, 11, 11a, 11b).

Regarding claim 55 Bereskin in view of Taniguchi et al. discloses a ground and line fault interrupter adapter module (See claim 23), comprising: a plurality of relay interconnects through-holes capable of receiving external electrical interconnects of an electrical circuit module (Taniguchi et al. – Fig. 8), a plurality of socket pins extending said adapter module, wherein said socket pins provide electrical communication between said external electrical interconnects and a socket (Taniguchi et al. – Abstract and Col. 1 line 64 to Col. 2 line 6), a plurality of bolt through-holes positioned proximate to the periphery of said adapter module, said through-holes receiving bolts that slide through, wherein said bolts secure said adapter module between said electrical circuit module and said socket (Taniguchi et al. – Fig. 6 <three modules on the right having holes to get secure to the panel, located at the upper left and bottom right corners), a ground and line fault interrupter circuitry (Bereskin – Abstract), including: a magnetic core (Bereskin – Fig. 1 element 36) surrounding said socket pins, said magnetic core detecting a magnetic field (Bereskin – Col. 2 lines 49-52 & Fig. 4) from the current flowing through said socket pins; multiple conductive windings wrapped around said magnetic core, said windings being arranged on said magnetic core to enable monitoring of the current flow through said socket pins (Bereskin – Fig. 1 elements 22w, 38), first and second sensing circuits electrically connected to said conductive winding, said sensing circuits detecting imbalances of the current flow between said socket pins and between at least one of said socket pins and ground (Bereskin – Col. 8 lines 59-68; Bereskin teaches about prior art using separated circuits for different fault detection <Col. 1 lines 24-32>), and a printed wiring board circuit breaker electrically connected with said first and second sensing circuits (Bereskin - Fig. 1 element 46<Col. 3 lines 12-13 intrinsically teaches about a electronic board>), said circuit breaker receiving a fault current from said sensing circuits, wherein said circuit breaker is tripped (Bereskin – Fig. 1 element 46) and generates an electronic fault signal when said received fault current exceeds a preset threshold (Bereskin does not specifically disclose thresholds and signals greater than or equal to that value to trip the circuit breaker. However, Bereskin teaches a voltage sensor that is designed such that a electromagnetic actuator is actuated, tripping a circuit breaker, only when the decrease in voltage across a neutral

winding drops to a level corresponding to a line conductor leakage path through resistor exceeding a certain value of current <Col. 6 lines 18-24>), wherein said generated electronic fault signal is sent to said electrical circuit module (Bereskin – Fig 1 elements 42, 44, 46).

Regarding claim 57 Bereskin in view of Taniguchi et al. discloses the ground and line fault interrupter adapter module of Claim 55.
Taniguchi et al. further discloses wherein said socket is mounted on a panel, and wherein said panel is in electrical communication with said socket and external electronic circuitry (Fig. 6).

Regarding claim 58 Bereskin in view of Taniguchi et al. discloses the ground and line fault interrupter adapter module of Claim 55.
Bereskin further discloses wherein said electrical circuit module includes a circuit breaker system (Fig. 1 element 46) and wherein said electronic fault signal (Fig. 1 signal sensed by element 42) activates said circuit breaker (Fig. 1 element 44) system to interrupt the power supply (Fig. 1 element 10) for a load (Fig. 1 element 30) electrically connected with said external electronic circuitry. Taniguchi et al. discloses circuit modules where the relays are plugged-in (Fig. 6 elements 30A).

Regarding claim 16 Bereskin discloses the module of claim 57.
Bereskin further discloses wherein said external electronic circuitry is in electrical communication with at least one of a fuel pump circuit, an engine circuit, and a gas pump circuit (Col. 1 lines 10-12).

Claim 17 is rejected under 35 U.S.C. §103(a) as being unpatentable over Bereskin (US 4159499) in view of Taniguchi et al. (US 5000692) and Langford et al. (US 6650516)

Regarding claim 17 Bereskin in view of Taniguchi et al. discloses the module of claim 57.

Bereskin in view of Taniguchi et al. does not disclose wherein said external electronic circuitry is positioned proximate to a flammable material.
Langford et al. teaches having the circuit reaching temperatures that can create fire hazard. It is implicitly determined flammable materials in the surroundings (Col. 1 lines 19-34).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin in view of Taniguchi et al. device with the Langford et al. teachings because a more secure device is obtained.

Claim 40 is rejected under 35 U.S.C. §103(a) as being unpatentable over Bereskin (US 4159499) in view of Loh (US 3801871).

Regarding claim 40 Bereskin discloses the method of claim 39.
Bereskin does not disclose wherein the step of filtering at least one of the line and ground fault signals includes a step of adjusting a frequency characteristic of an electronic filter to obtain a desired filter characteristic.
Loh teaches wherein the step of filtering at least one of the line and ground fault signals includes a step of adjusting a frequency characteristic of an electronic filter to obtain a desired filter characteristic (Col. 2 lines 20-25).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the Loh teachings because a more secure and sophisticated device is obtained, which adjust to the frequency of the faults.

Claim 45 is rejected under 35 U.S.C. §103(a) as being unpatentable over Bereskin (US 4159499) in view of E. L. Harder (US 2809330).

Regarding claim 45 Bereskin discloses the ground and line fault interrupter of Claim 44.

Bereskin does not disclose wherein said circuit breaker detector is a printed wiring board circuit breaker set to trip on a lower current draw than said circuit breaker of said external circuit breaker system.
E. L. Harder teaches wherein said circuit breaker detector is a printed wiring board circuit breaker set to trip on a lower current draw than said circuit breaker of said external circuit breaker system (Col. 9 lines 57-62).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the E. L. Harder teachings because it provides the possibility of using equipment having an extremely low power consumption, which obviates the necessity for fuses in the secondary wiring-circuits, or control-circuit breakers.

Claims 47 & 48 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bereskin (US 4159499) in view of Engel et al. (US 5963405).

Regarding claim 47 Bereskin the ground and line fault interrupter of Claim 43.
Bereskin further discloses wherein said first sensing circuit includes an impedance electrically connected to a comparator through an electronic filter and rectifier, wherein said impedance is a load that provides a voltage drop which is rectified and filtered (Col. 8 lines 47-68).
Bereskin does not disclose wherein the characteristics of said filter are adjusted to balance a trip time with a number of false trips.
Engel et al. teaches wherein the characteristics of said filter are adjusted to balance a trip time with a number of false trips (Abstract).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the Engel et al. teachings because a more secure and sophisticated device is obtained, which adjust to the frequency of the faults and trips only when really needed.

Regarding claim 48 Bereskin the ground and line fault interrupter of Claim 43. Bereskin further discloses wherein said second sensing circuit includes an impedance electrically connected to a comparator through an electronic filter and rectifier, wherein said impedance is a load that provides a voltage drop which is rectified and filtered, and wherein the characteristics of said filter are adjusted to balance a trip time with a number of false trips (Col. 8 lines 47-68).
Engel et al. teaches wherein the characteristics of said filter are adjusted to balance a trip time with a number of false trips (Abstract).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the Engel et al. teachings because a more secure and sophisticated device is obtained, which adjust to the frequency of the faults and trips only when really needed.

Claim 49 is rejected under 35 U.S.C. §103(a) as being unpatentable over Bereskin (US 4159499) in view of O. C. Traver (US 1919969).

Regarding claim 49 Bereskin discloses the ground and line fault interrupter of Claim 43.
Bereskin does not specifically discloses wherein said conductive windings are summed together to provide a first output voltage that is proportional to a ground fault level to said first sensing circuit and to provide a second output voltage that is proportional to a line fault level to said second sensing circuit
Bereskin teaches about prior art using separated circuits for different fault detection (Col. 1 lines 24-32).
O. C. Traver teaches summing the windings (current faults thru them) (Page 4 lines 117-123).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin device with the O. C. Traver teachings because a more secure and capable of preventing instability.

Claims 51, 54 & 56 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bereskin (US 4159499) in view of Taniguchi et al. (US 5000692) and Blades (US 5434509).

Regarding claim 51 Bereskin in view of Taniguchi et al. discloses the ground and line fault interrupter of Claim 43.
Bereskin in view of Taniguchi et al. does not disclose wherein including a test circuit, wherein said test circuit is electrically connected to said conductive windings and enables manual input of a fault current.
Blades teaches wherein including a test circuit, wherein said test circuit is electrically connected to said conductive windings and enables manual input of a fault current (Col. 25 lines 31-37).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin in view of Taniguchi et al. device with the Blades device because this feature allows to check if the device is properly functioning.

Regarding claim 54 Bereskin in view of Taniguchi et al. discloses the ground and line fault interrupter of Claim 43.
Bereskin in view of Taniguchi et al. does not disclose wherein including a reset circuit electrically connected to said circuit breaker detector, wherein said reset circuit enables the manual reset of said circuit breaker detector if tripped.
Blades teaches wherein including a reset circuit electrically connected to said circuit breaker detector, wherein said reset circuit enables the manual reset of said circuit breaker detector if tripped (Col. 25 lines 31-37).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin in view of Taniguchi et al. device with the Blades device because this feature allows to reset the device which has been falsely tripped.

Regarding claim 56 Bereskin in view of Taniguchi et al. discloses the ground and line fault interrupter of Claim 55.

Bereskin in view of Taniguchi et al. does not disclose wherein including a test circuit electronically connected to said conductive windings and reset circuit electronically connected to said circuit breaker and wherein said adapter module includes a control circuit panel providing control switches for said test and reset circuits.

Blades teaches wherein including a test circuit electronically connected to said conductive windings and reset circuit electronically connected to said circuit breaker (Col. 25 lines 31-37) and wherein said adapter module includes a control circuit panel providing control switches for said test and reset circuits (Fig. 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Bereskin in view of Taniguchi et al. device with the Blades device because this feature allows to manually activate the test switch to check if the device is properly functioning and reset the reset switch to reset the device which has been falsely tripped.

Response to Arguments

Applicant's arguments have been given carefully consideration but they are now moot in view of new grounds of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luis E. Román whose telephone number is (571) 272 – 5527. The examiner can normally be reached on Mon – Fri from 7:15 AM to 3:45 PM.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800 x 36. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
Information regarding the status of an application may be obtained from Patent Application Information Retrieval (PAIR) system.

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LR/020606

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